FRC.005RC2

PATENT 2/864

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Xpplicant

Peter Warnes, et al.

Appl. No.

09/523,877

Filed

March 13, 2000

For

METHOD AND APPARATUS FOR MULTI-MODE JUMP

DELAY SLOT CONTROL IN A PIPELINED PROCESSOR

Examiner

Huisman, David J.

Group Art Unit:

2183

27299

PATENT .TRADEMARK OFFICE

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

April 1, 2005

(Date)

Robert F. Gazdzinski, Reg. No. 39,990

TRANSMITTAL LETTER

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

- 1. Information Disclosure Statement citing twenty-three (23) references (2 pages);
- 2. Form PTO-1449 enclosing twenty-three (23) references (1 page);
- 3. Check in the sum of \$180.00; and
- 4. Return prepaid postcard.

Respectfully submitted, GAZDZINSKI & ASSOCIATES

Dated: 4/1/8

By: <

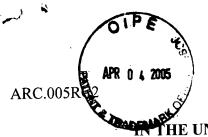
Robert F. Gazdzinski, Esq. Registration No. 39,990

Attorney of Record

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NITED STATES PATENT AND TRADEMARK OFFICE

Peter Warnes, et al. **Applicant** 09/523,877 Appl. No. ATENT TRADEMARK OFFICE March 13, 2000 Filed METHOD AND APPARATUS FOR For MULTI-MODE JUMP DELAY SLOT CONTROL IN A PIPELINED **PROCESSOR** Huisman, David J. Examiner 2183 Group Art Unit:

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing twenty-three (23) references that are also enclosed. This Information Disclosure Statement is being filed before the mailing date of either a final action under 37 C.F.R. § 1.113, or a notice of allowance under 37 C.F.R. § 1.311, whichever occurs first, and is accompanied by the fee set forth in 37 C.F.R. § 1.17(p).

first, and is accompanied by the fee set forth in 37 C.F.R. § 1.17(p).

Pursuant to 37 C.F.R. § 1.97(g) and (h), Applicant makes no representation that a search has been made or that the information cited is considered to be material to patentability. Additionally, inclusion on this list is not an admission that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that any of the cited documents are prior so that are App. No.

09/523,877

Filed

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March 13, 2000

art in this application. Further, Applicant makes no representation regarding the completeness of this list or that better art does not exist.

The Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 and § 1.17 which may be required to Deposit Account No. 501423. This sheet is attached in duplicate.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: 4/1/03

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| | FORM PTO-1449 |
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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

| COMMERCE | ATTY. DOCKET NO. |
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| ARK OFFICE | ARC.005RC2 |

APPLICATION NO. 09/523,877

RMATION DISCLOSURE STATEMENT
BY APPLICANT

SEVERAL SHEETS IF NECESSARY)

APPLICANT Peter Warnes, et al.

FILING DATE March 13, 2000 GROUP 2183

| | | | | U.S. PATENT DOCUMENTS | | | |
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| | 20 | Tensilica, Inc; Xtensa Instruction Set Architecture (ISA) Reference Manual Revision 1.0. (First 25 pages) |
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| | 22 | Compton et al., "Configurable Computing: A Survey of Systems and Software," Technical Report, Northwestern University, Dept. of ECE, 1999. |
| | 23 | Yang, Jin-Hyuk, et al., "MetaCore: A Configurable & Instruction-Level Extensible DSP Core," Proceedings of the ASP-DAC '98 Asian and South Pacific Design Automation Conference 1998, pages 325-326, XP-002137268 |

DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.